AMENDMENTS TO THE CLAIMS

1. (currently amended) A non-volatile synchronous memory device comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of non-volatile memory cells; and

a plurality of bank buffers, the bank buffers and addressable banks coupled one to one ~~coupled to each of the plurality of addressable banks~~, wherein each of the plurality of bank buffers ~~comprises bits~~ is adapted to store data from a row of memory cells contained in ~~a~~ its corresponding addressable bank of the plurality of addressable banks.

2. (original) The non-volatile synchronous memory device of claim 1 wherein the plurality of addressable banks comprise four addressable banks.

3. (original) The non-volatile synchronous memory device of claim 1 further comprising control circuitry to copy data from a first row of a first bank of the plurality of addressable banks to a first buffer of the plurality of buffers.

4. (original) The non-volatile synchronous memory device of claim 3 wherein an address of the first row is predefined and the control circuitry copies the data in response to an externally provided command.

5. (original) The non-volatile synchronous memory device of claim 1 wherein the plurality of buffers can be read while data is written to the plurality of banks.

6. (currently amended) A processing system comprising:

a processor; and

a non-volatile synchronous memory device coupled to the processor and comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of non-volatile memory cells, and

a plurality of bank buffers, the bank buffers and addressable banks coupled one to one ~~coupled to each of the plurality of addressable banks~~, wherein each of the plurality of bank buffers ~~comprises bits~~ is adapted to store data from a row of memory cells contained in ~~a~~ its corresponding addressable bank of the plurality of addressable banks.

7. (original) The processing system of claim 6 wherein the plurality of addressable banks comprise four addressable banks.

8. (original) The processing system of claim 6 wherein the non-volatile synchronous memory device further comprises control circuitry to copy data from a first row of a first bank of the plurality of addressable banks to a first buffer of the plurality of buffers.

9. (original) The processing system of claim 8 wherein an address of the first row is predefined and the control circuitry copies the data in response to an externally provided command.

10. (original) The processing system of claim 6 wherein the plurality of buffers can be read while data is written to the plurality of banks.

11. (currently amended) A method of writing to a flash memory comprising:

copying first data stored in a row of a first non-volatile memory cell array bank to a first buffer circuit using control circuitry of the flash memory;

copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit using the control circuitry;

performing a write operation to write ~~second~~ third data to the first array bank using a first external processor coupled to the flash memory; ~~and~~

reading the first data from the first buffer circuit using the first external processor while performing the write operation; and

reading the second data from the second array bank using a second external processor coupled to the flash memory while performing the write operation.

12. (original) The method of claim 11 further comprising:

monitoring a status of the flash memory to determine when the write operation is completed.

13. (currently amended) The method of claim 12 wherein monitoring is performed by ~~an~~ the first external processor in response to the first data read from the buffer circuit.

14. (currently amended) The method of claim 11 wherein copying the first data is initiated by ~~an~~ the first external processor coupled to the flash memory.

15. (currently amended) The method of claim 11 wherein copying the first data and performing the write operation is initiated by ~~an~~ the first external processor coupled to the flash memory.

16. (currently amended) A method of operating a flash memory comprising:

copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory;

performing a write operation to write second data to the first array bank using an external processor coupled to the flash memory in response to ~~an~~ the external processor ~~coupled to the flash memory~~;

reading the first data from the buffer circuit using the external processor while performing the write operation, wherein the first data contains instruction code for the processor; and

monitoring the write operation with the external processor in response to the instruction code.

17. (original) The method of claim 16 wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.

18. (currently amended) The method of claim 16 further comprises reading third data from a second array bank with a second external processor while performing the write operation.

19. (currently amended) The method of claim 16 wherein copying first data to the buffer circuit is automatically performed by ~~flash memory~~ the control circuitry in response to an externally provided write command.

20. (currently amended) The method of claim 16 wherein copying first data to the buffer circuit is performed in response to an externally provided command from the external processor.

21. (currently amended) A method of operating a flash memory comprising:

copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to a command from an external processor coupled to the flash memory;

performing a write operation to write second data to a second row of the first array bank using the external processor in response to a write command provided by the processor;

reading the first data from the buffer circuit using the external processor while performing the write operation in response to a read command provided by the processor, wherein the first data contains instruction code for the external processor; and

monitoring a status register of the flash memory with the external processor in response to the instruction code.

22. (currently amended) The method of claim 21 further comprises reading third data from a second array bank with a second external processor while performing the write operation.

23. (currently amended) A method of operating a flash memory comprising:

receiving a write command ~~with~~ at the flash memory, wherein the write command is provided by an external processor coupled to the flash memory;

automatically copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to the write command;

performing a write operation to write second data to a second row of the first array bank using the external processor in response to a write command provided by the processor;

reading the first data from the buffer circuit using the external processor while performing the write operation in response to a read command provided by the external processor, wherein the first data contains instruction code for the external processor; and

monitoring a status register of the flash memory with the external processor in response to the instruction code.

24. (currently amended) The method of claim 23 further comprises reading third data from a second array bank with a second external processor while performing the write operation.

25. (currently amended) A method of operating a synchronous flash memory comprising:

storing instruction code in each of a plurality of array blocks of the synchronous flash memory; and

copying the instruction code from a first array block to a buffer circuit using control circuitry of the memory, during a write operation, to the first array block using an

external processor coupled to the memory so that the instruction code can be read from the buffer circuit using the external processor during the write operation.

26. (original) The method of claim 25 wherein the synchronous flash memory comprises four array blocks.

27. (original) The method of claim 25 wherein copying the instruction code is performed in response to an externally provided write command.